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PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Add PCIe 2.0 Signaling and Functionality
DATE:	Updated March 17, 2009
AFFECTED DOCUMENT:	PCI Express Mini Card Electromechanical Specification Revision 1.2
SPONSOR:	Caldwell Crosswy, Hewlett-Packard

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Part I

1. Summary of the Functional Changes

This ECR updates the PCIe Mini CEM specification to incorporate PCIe Base Specification 2.0. This would nominally take the Mini CEM spec to the 2.0 level.

2. Benefits as a Result of the Changes

The current version of the PCIe Mini Card specification is limited to PCIe 1.x data rates. Functions are emerging that can leverage the higher data rate inherent in the PCIe 2.0 Base Specification.

By incorporating (referencing) the PCIe 2.0 Base Specification into the Mini Card spec, this ECR adds the 5.0Gbps signaling rate (and other functionality) of the PCIe 2.0 Base Specification to the PCIe Mini Form Factor.

3. Assessment of the Impact

Minimal impact expected. Key work item for the Working Group will be to undertake characterization of the current Mini Card connector at 2.0 (5.0Gbps) signaling rates.

4. Analysis of the Hardware Implications

No changes are expected to the pin definitions.

5. Analysis of the Software Implications

No software implications are expected.

6. Analysis of the C&I Test Implications

N/A

Part II – Detailed Description of the changes

Change Section 1.1 as follows:

1.1. Overview

This specification defines an implementation for small form factor PCI Express cards. The specification uses a qualified sub-set of the same signal protocol, electrical definitions, and configuration definitions as the *PCI Express Base Specification, Revision 2.0*. Where this specification does not explicitly define PCI Express characteristics, the *PCI Express Base Specification* governs.

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Change Section 1.2 as follows:

1.2. Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- *PCI Express Base Specification, Revision 2.0*
- *PCI Express Card Electromechanical Specification, Revision 2.0*

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Change Section 3.4.2 as follows:

3.4.2. Digital Interfaces

Signal integrity requirements are defined separately for 2.5 Gbps and 5.0 Gbps applications. Mini Card sockets that are designed for 5.0 Gbps applications shall also be useable with Mini Cards that only operate up to 2.5 Gbps.

3.4.2.1. Signal Integrity Requirements and Test Procedures for 2.5 Gbps Support

A common electrical test fixture is specified and used for evaluating connector signal integrity. The test fixture has 50 Ω single ended traces 0.1524 mm (6 mils) wide that must be uncoupled. The impedance variation of those traces shall be controlled within ±5%. Refer to Appendix A for detailed discussions on the test fixture.

Detailed testing procedures, such as the vector network analyzer settings, operation, and calibration are specified in Appendix A. This appendix should be used in conjunction with the PCI Express Connector Test Fixture.

For the insertion loss and return loss tests, the measurement shall include 1-inch long PCB traces with 0.5 inches on the system board and 0.5 inches on the add-in card. Note that the edge finger pad is not counted as the add-in card PCB trace. It is considered part of the connector interface. The 1-inch PCB trace included in the connector measurement is a part of the trace length allowed on the system board.

Either single ended measurements that are processed to extract the differential characteristics or true differential measurements are allowed. The detailed definition and description of the test fixture and the measurement procedures are provided separately in Appendix A.

An additional consideration to the connector electrical performance is the connector-to-system board and connector-to-add-in-card launches. The connector through hole pad and anti-pad sizes, as well as trace layout on the system board shall follow the recommendations in the *PCI Express Electrical Design Guidelines*. On the add-in card, the ground and power planes underneath the PCI Express high-speed signals (edge fingers) shall be removed. Otherwise, the edge fingers will have too much capacitance and greatly degrade the connector performance. More detailed discussion on the add-in card electrical design can be found in Appendix A and *PCI Express Electrical Design Guidelines*.

Table 3-8 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 3-8: Signal Integrity Requirements and Test Procedures for 2.5 Gbps

Parameter	Procedure	Requirements
Differential Insertion loss (DDIL)	EIA 364-101 The EIA standard must be used with the following considerations: 1. The step-by-step measurement procedure is outlined in Appendix A. 2. A common test fixture for connector characterization will be used. 3. This is a differential insertion loss requirement. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so is covered in Appendix A.	≤1 dB up to 1.25 GHz; ≤ [1.6 * (F - 1.25)+1] dB for 1.25 GHz < f ≤ 3.75 GHz (for example, ≤5 dB at f = 3.75 GHz)
Differential Return loss (DDRL)	EIA 364-108 The EIA standard must be used with the following considerations: 1. The step-by-step measurement procedure is outlined in Appendix A. 2. A common test fixture for connector characterization will be used. 3. This is a differential return loss requirement. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential characteristics of the connector. The	≤ -12 dB up to 1.3 GHz; ≤ -7 dB for 1.3 GHz < f ≤ 2 GHz; ≤ -4 dB for 2 GHz < f ≤ 3.75 GHz

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	methodology of doing so is covered in Appendix A.	
Intra-pair skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. This is reflected in the measurement procedure and adjustments to the procedure should be made accordingly. 2. The step-by-step measurement procedure is outlined in Appendix A. 3. A common test fixture for connector characterization will be used. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential crosstalk of the connector. The methodology of doing so is covered in Appendix A.	≤ -32 dB up to 1.25 GHz; ≤ -[32 - 2.4 * (f - 1.25)] dB for 1.25 GHz < f ≤ 3.75 GHz (for example, ≤ -26 dB at f = 3.75 GHz)
Jitter	By design; measurement not required	10 ps max

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Notes:

1. A network analyzer is preferred. If greater dynamic range is required, a signal generator/spectrum analyzer may be used. Differential measurements require the use of a two-port (or a four-port) network analyzer to measure the connector. The differential parameters may be measured directly if the equipment supports “True” differential excitation. (“True” differential excitation is the simultaneous application of a signal to one line of the pair and a 180-degree phase shifted version of the signal to the second line of the pair.) If single ended measurements are made, the differential connector parameters must be derived from the single ended measurements as defined in Appendix A.
2. If differential measurements are made directly by application of differential signals, the equipment must use phase-matched fixturing. The fixturing skew and measurement cabling should be verified to be < 1 ps on a TDR.
3. The connector shall be targeted for a 100 Ω differential impedance, though it is not explicitly specified.

3.4.2.2. Signal Integrity Requirements and Test Procedures for 5.0 Gbps Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are de-embeded from measurements. Test fixture requirements and recommendations are also included in this section.

Table 3-x lists the electrical signal integrity parameters, requirements, and test procedures.

Table 3-x: Signal Integrity Requirements and Test Procedures for 5 Gbps

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 ohm differential impedance. 2. The test fixture shall meet the test fixture requirement defined further in this section. The test fixture effect shall be removed from the measured S parameters. Refer to Note 1.	≥ -0.5 dB up to 2.5 GHz; ≥ -[0.8*(f-2.5)+0.5] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥-2.5 dB at f = 5 GHz); ≥ -[3.0*(f-5)+2.5] dB for 5 GHz < f ≤ 7.5 GHz (for example, ≥-10 dB at f = 7.5 GHz);
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 ohms differential impedance. 2. The test fixture shall meet the test fixture requirement in further in this section. The test fixture effect shall be removed. Refer to Note 1.	≤ -15 dB up to 3.0 GHz; ≤ -5 dB for 3.0 GHz < f ≤ 5 GHz; ≤ -1 dB for 5.0 GHz < f ≤ 7.5 GHz.
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 ohm differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5.0 GHz; ≤ -20 dB for 5.0 GHz < f ≤ 7.5 GHz;

Notes:

1. The specified S parameters requirements are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

The test fixture for connecter S-parameter measurement should be designed and built to the following requirements:

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The test fixture shall be an FR4-based PCB of the micro-strip structure; the dielectric thickness or stack-up shall be approximately .102 mm (4 mils).

The total thickness of the test fixture PCB shall be 1.57 mm (0.62") and the test add-in card should be a break-out card fabricated in the same PCB panel for the fixture.

The measurement signals shall be launched into the connector from the top of the test fixture, capturing the through-hole stub effect.

Traces between the connector and measurement ports (SMA or microprobe) should be uncoupled.

The trace lengths between the connector and measurement port shall be minimized. The maximum trace length shall not exceed 45.72 mm (1800 mils). The trace lengths between the connector and measurement port on the test baseboard and add-in card shall be equal. Note that the edge finger pad is not counted as the add-in card PCB trace; it is considered as a part of the connector interface.

All of the traces on the test board and add-in card must be held to a characteristic impedance of 50 Ohms with a tolerance of +/- 7%.

The test add-in card edge finger pads shall be fabricated per mechanical requirements defined in this specification. The ground plane immediately underneath the edge finger pads must be removed.

The through-hole on the test board shall have the following stack-up: .711 mm (28 mil) finished hole, 1.067 mm (42 mil) pad, and 1.473 mm (58 mil) anti-pad.

Use of SMA connectors is recommended. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 60 ps rise time is recommended to be within 50+/-7 ohms. If a fixture with other characteristics is used, the fixture effects must be reliably removed and must not impact measurement accuracy.

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